BURR - BROWN®

3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

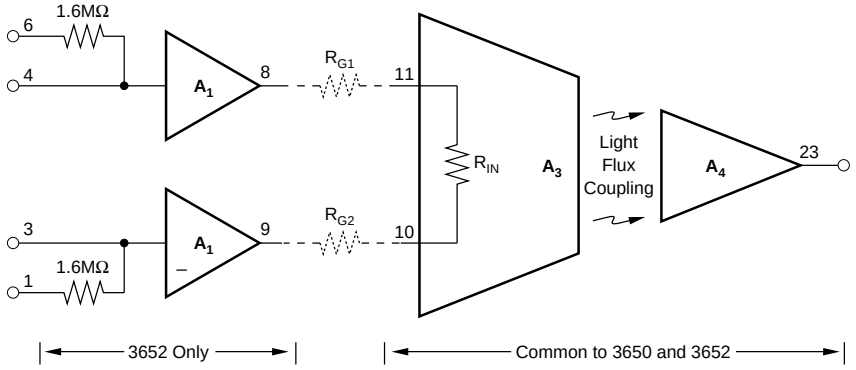
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES:
  ±2000V Continuous
  140dB Rejection
- ULTRA LOW LEAKAGE:
  0.35μA max at 240V/60Hz
  1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY:
  0.05% Linearity
  0.05%/1000 Hrs Stability
- WIDE BANDWIDTH:
  15kHz ±3dB
  1.2V/μs Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers, the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier-type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



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SBOS129

SPECIFICATIONS

At +25°C and ±15VDC supply voltages, unless otherwise specified.

PRODUCT	3650MG, HG[1]	3650JG	3650KG	3652MG, HG[1]	3652JG
ISOLATION					
Isolation Voltage					
Rated Continuous, min	2000Vp or VDC				
Tested Voltage, min, 10s Duration	5000Vp				
Isolation Mode Rejection, G = 10					
DC	140dB				
60Hz, 5000Ω Source Unbalance	120dB				
Leakage Current, 240V/60Hz	0.35µA, max				
Isolation Impedance					
Capacitance	1.8pF				
Resistance	$10^{12}\Omega$				
GAIN					
Gain Equation					
for Current Sources	$G_1 = 10^6$V/Amp			$G_1 = 1.0057 \times 10^6$V/Amp[2]	
for Voltage Sources	$G_V1 = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V			$\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max	25Ω			25Ω	
Buffer Output Impedance, R_O	Not Applicable			90Ω ±30Ω	
Gain Equation Error, max[3]	1.5%	0.5%	0.5%	1.5%[4]	0.5%[4]
Gain Nonlinearity	±0.05% typ ±0.2% max	±0.03% typ ±0.1% max	±0.02% typ ±0.05% max	±0.05% typ ±0.2% max	±0.05% typ ±0.1% max
Gain vs Temperature	300ppm/°C	100ppm/°C	50ppm/°C	300ppm/°C	200ppm/°C
Gain vs Time	±0.05%/1000hrs			±0.05%/1000hrs	
Frequency Response					
Slew Rate	0.7V/µs min, 1.2V/µs typ				
±3dB Frequency	15kHz				
Settling Time					
to ±0.01%	400µs				
to ±0.1%	200µs				
INPUT STAGE[5]					
Input Offset Voltage					
at 25°C, max[3]	±5mV	±1mV	±0.5mV	±5mV	±2mV
vs Temperature, max	±25µV/°C	±10µV/°C	±5µV/°C	±50µV/°C	±25µV/°C
vs Supply	100µV/V			100µV/V	
vs Time	50µV/1000hrs			100µV/1000hrs	
Input Bias Current					
at 25°C	10nA typ, 40nA max			10pA typ, 50pA max	
vs Temperature	0.3nA/°C			Doubles Every +10°C	
vs Supply	0.2nA/V			1pA/V	
Input Offset Current				10pA	
vs Temperature	Effects Included			Doubles Every +10°C	
vs Supply	In Output Offset			1pA/V	
Input Impedance					
Differential	"R_{IN}" = 25Ω max			$10^{11}\Omega$	
Common-Mode	$10^9\Omega$			$10^{11}\Omega$	
Input Noise					
Voltage, 0.05Hz to 100Hz	4µVp-p			8µVp-p	
10Hz to 10kHz	4µVrms			5µVrms	
Input Voltage Range					
Common-Mode, Linear Operation,	±(|V| –5)V			±(|V| –5)	
w/o damage, at +, –	±V			±V	
at +I, –I	Not Applicable[6]			±300V for 10ms[7]	
at $+I_R$, $-I_R$	Not Applicable[6]			±3000V for 10ms[7]	
Differential, w/o damage, at +, –	±V			±V	
Differential, w/o damage, at +I, –I	Not Applicable			±600V for 10ms[7]	
Differential, w/o damage,					
at $+I_R$, $-I_R$	Not Applicable			±6000V for 10ms[7]	
Common-Mode Rejection, 60Hz	90dB at 60Hz, 5kΩ Imbalance			80dB at 60Hz, 5kΩ Imbalance	
Power Supply (Input Stage Only)					
Voltage (at "+V" and "–V")	±8V to ±18V			±8V to ±18V	
Current					
Quiescent	±1.2mA[8]			±3mA[8]	
with ±10V Output[7]	+6.5mA or –6.5mA, typ			+8.5mA or –8.5mA, typ	
	+12mA or –12mA, max			+16mA, or –16mA, max	

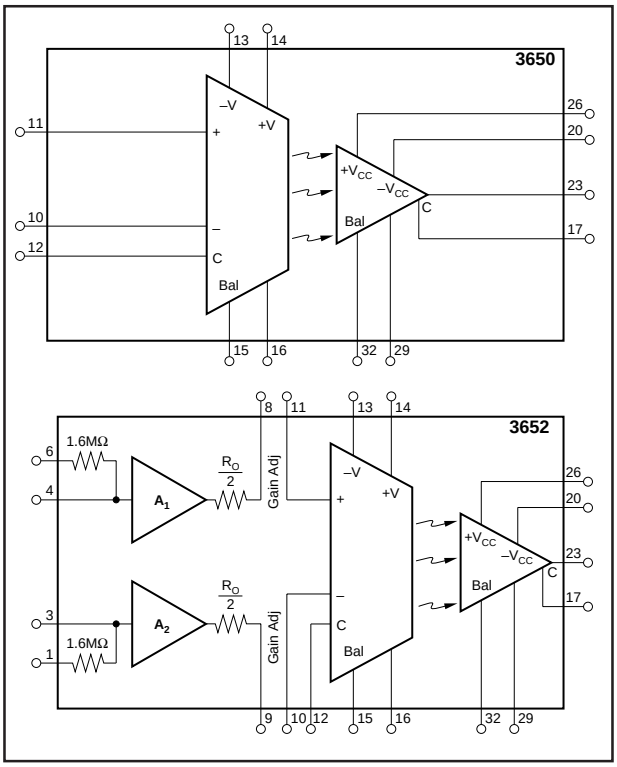
SPECIFICATIONS (CONT)

At +25°C and ±15VDC supply voltages, unless otherwise specified.

PRODUCT	3650MG, HG[1]	3650JG	3650KG	3652MG, HG[1]	3652JG
OUTPUT STAGE					
Output Voltage, min	±10V			±10V	
Output Current, min	±5mA			±5mA	
Output Offset Voltage					
at 25°C, max[3]	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900µV/°C	±450µV/°C	±300µV/°C	±900µV/°C	±450µV/°C
vs Supply		±500µV/V		±500µV/V	
vs Time		±1mV/1000hrs		±1mV/1000hrs	
Output Noise Voltage					
0.05Hz to 100Hz		50µVp-p		50µVp-p	
10Hz to 1kHz		65µVrms		65µVrms	
Power Supply (Output Stage Only)					
Voltage ("+V_{CC}" and "–V_{CC}")	±8V to ±18V				
Current					
Quiescent	±2.3mA typ, ±6mA max				
with ±5mA Output, max	±11mA				
TEMPERATURE[9]					
Specification	0°c to +85°C				
Operating	–40°C to +100°C				
Storage	–40°C to +125°C				

NOTES: (1) All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration increased from 10 seconds minimum to 60 seconds minimum; (b) Input offset voltage at 25°C, max: ±10mV; vs temperature max: ±100µV/°C; (c) Output offset voltage at 25°C, max; ±50mV; vs temperature max; ±1.8mV/°C. (2) If used as 3650, see Installation and Operating Instructions. (3) Trimmable to zero. (4) Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±1 or ±I_R pins). (5) Input stage specifications at +I and –I inputs for 3652 unless otherwise noted. (6) Maximum safe input current at either input is 10mA. (7) Continuous rating is 1/3 pulse rating. (8) Load current is drawn from one supply lead at a time: other supply current at quiescent level. For 3652 add 0.2mA/V of positive CMV. (9) dT/dt < 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range.

PIN CONFIGURATIONS



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
3650	32-Pin DIP	77
3652	32-Pin DIP	77

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

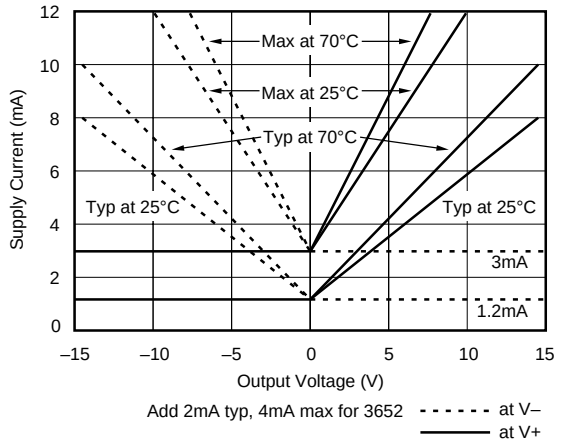
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

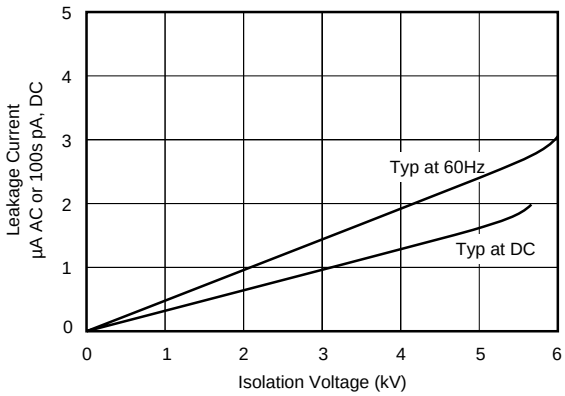
TYPICAL PERFORMANCE CURVES

Typical at +25°C and ±15VDC power supplies, unless otherwise noted.

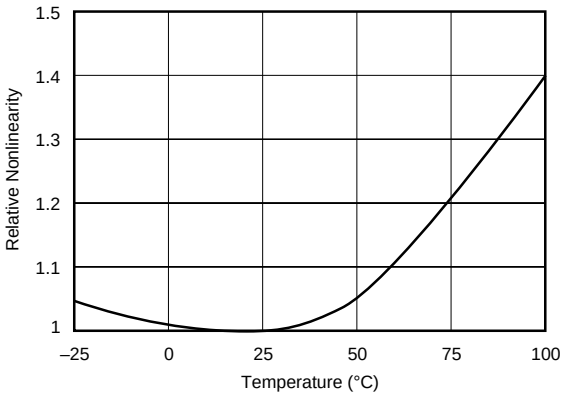
INPUT STAGE SUPPLY CURRENT
vs OUTPUT VOLTAGE



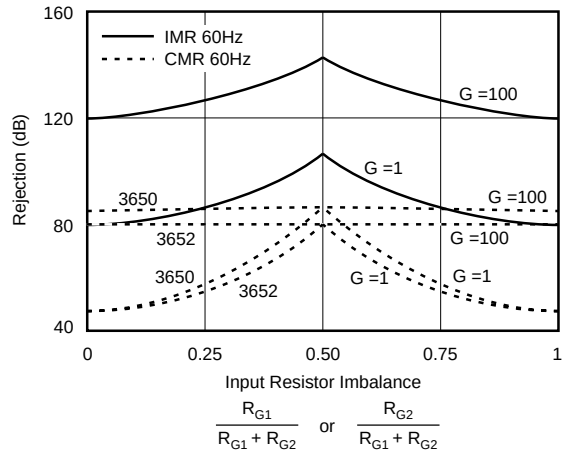
ISOLATION LEAKAGE CURRENT
vs ISOLATION VOLTAGE



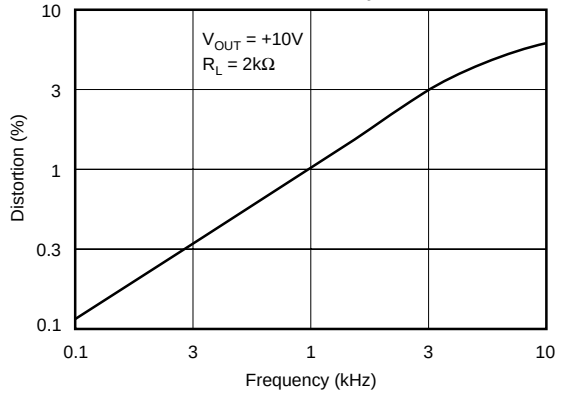
NORMALIZED LINEARITY vs TEMPERATURE



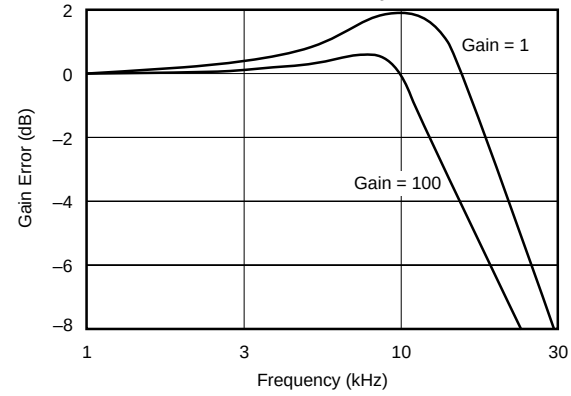
REJECTION vs RESISTOR IMBALANCE



DISTORTION vs FREQUENCY



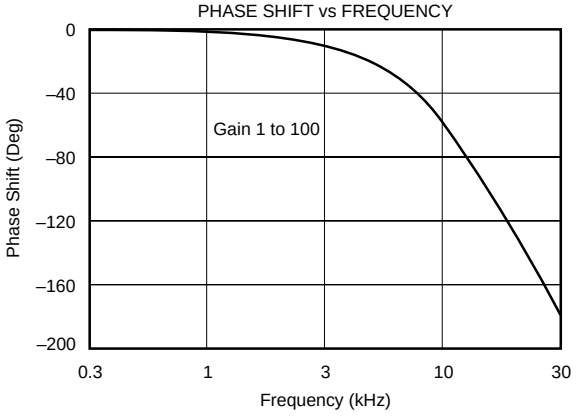
GAIN ERROR vs FREQUENCY



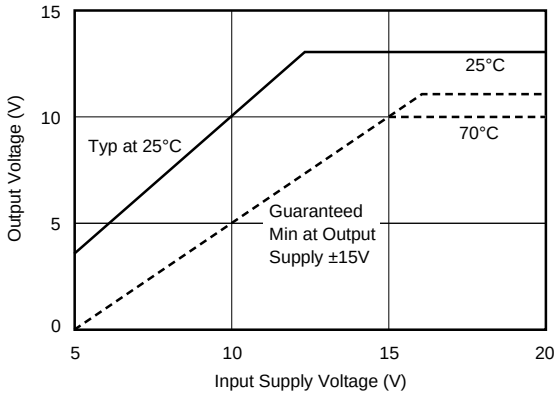
TYPICAL PERFORMANCE CURVES (CONT)

Typical at +25°C and ±15VDC power supplies, unless otherwise noted.

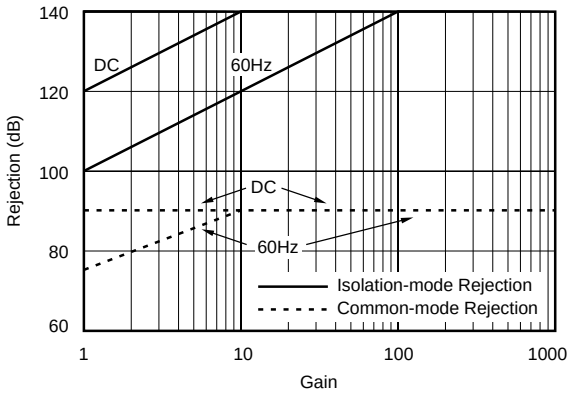
PHASE SHIFT vs FREQUENCY



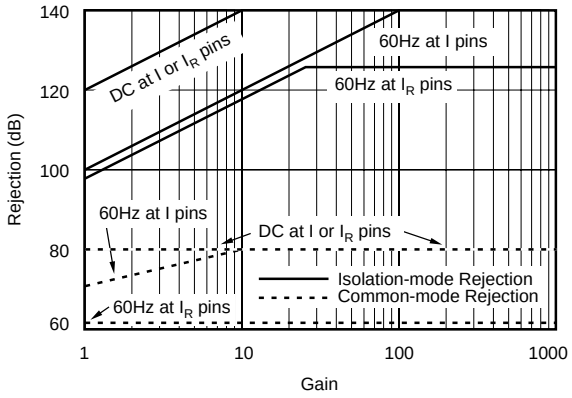
OUTPUT VOLTAGE SWING
vs INPUT SUPPLY VOLTAGE



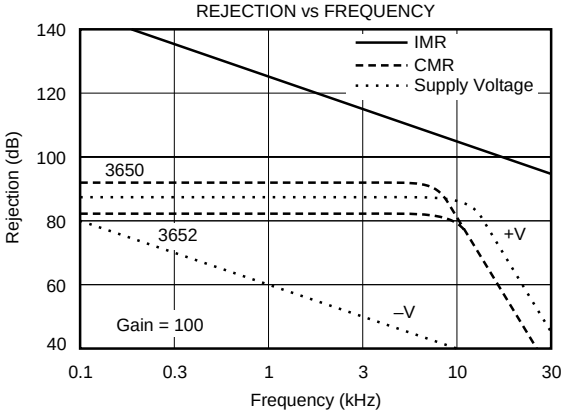
3650 COMMON-MODE AND
ISOLATION-MODE REJECTION vs GAIN



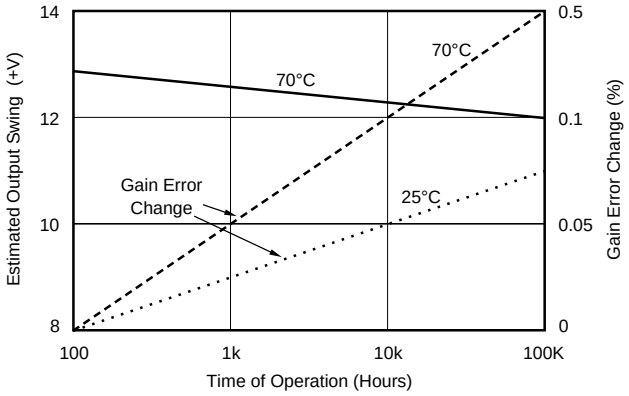
3652 COMMON-MODE AND
ISOLATION-MODE REJECTION vs GAIN



REJECTION vs FREQUENCY



OUTPUT VOLTAGE AND GAIN ERROR vs TIME



DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications: "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is a generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and 3652, the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V, each unit is tested at 5000V.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 1, $(V_+ + V_-)/2 = V_{CM}$. (NOTE: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

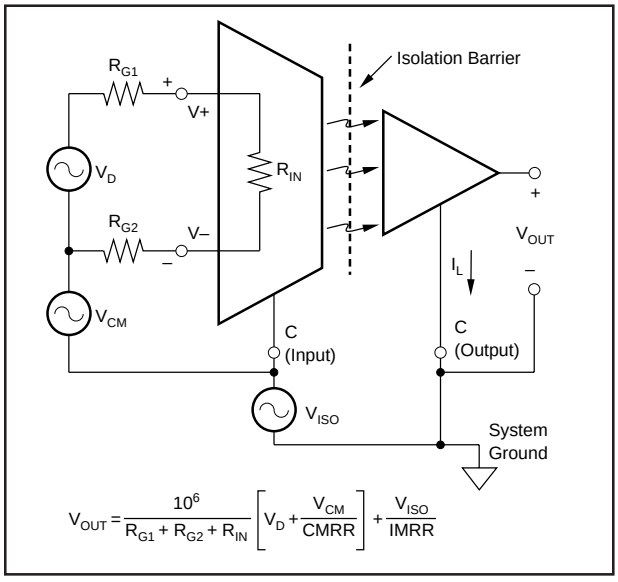


FIGURE 1. Illustration of Isolation-Mode and Common-Mode Specifications.

NOTE: (1) The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output (i.e. ±10mV at 20Vp-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations—primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650, which can be used to understand the basic operation without considering the cluttering details of offset adjustment and biasing for bipolar operation.

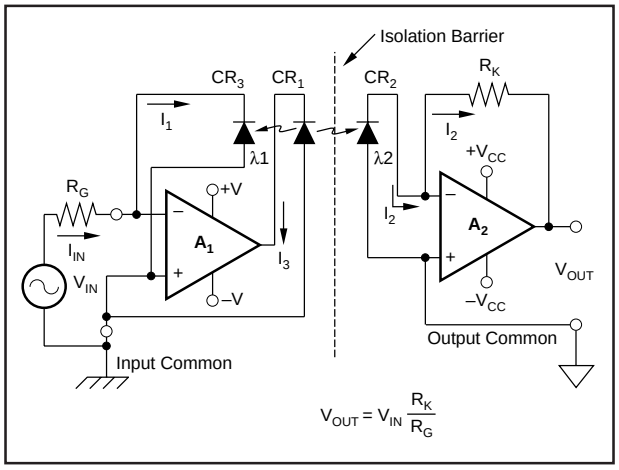


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used—one in the input (CR_3) and one in the output stage (CR_2)—to greatly reduce nonlinearities and time-temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{IN} R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched, and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{IN}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{OUT} = I_2 R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{OUT} = V_{IN} \frac{10^6}{R_G}, \ (R_G \text{ in } \Omega\text{s})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched(1). Linearity is now a

function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_D, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used, the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{IN} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

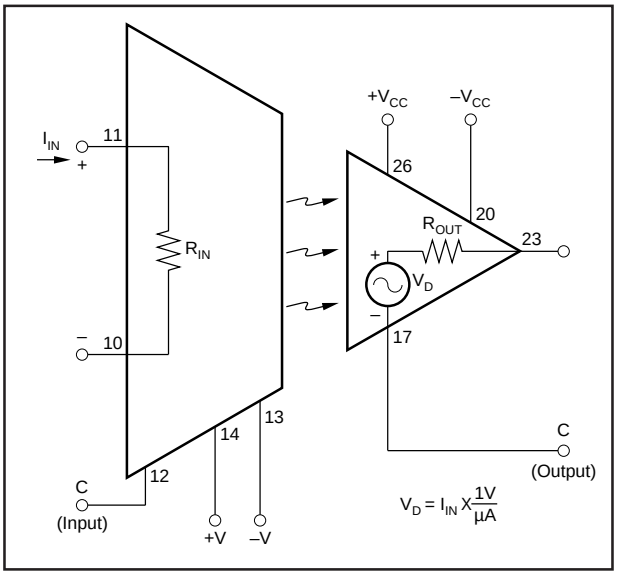


FIGURE 3. Simple Model of 3650.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The $+I_R$ and $-I_R$ inputs have a 10ms pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC/DC converter is used for isolated power, it is placed in parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC/DC converter such as the Burr-Brown Model 722 should be used.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used: the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains, (>10).

Use the following procedure if it is desired to null both input and output components. (For example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

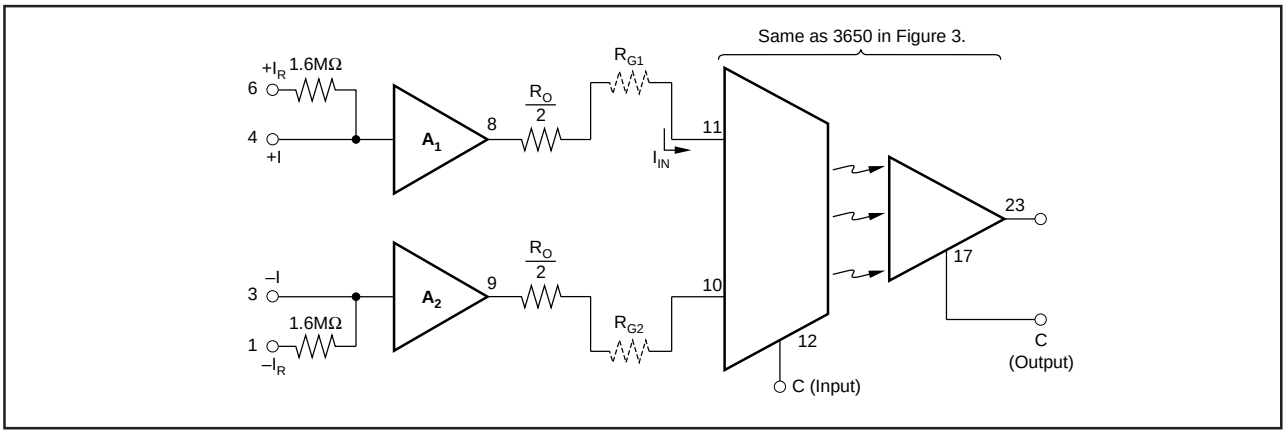


FIGURE 4. Simple Model of 3652.

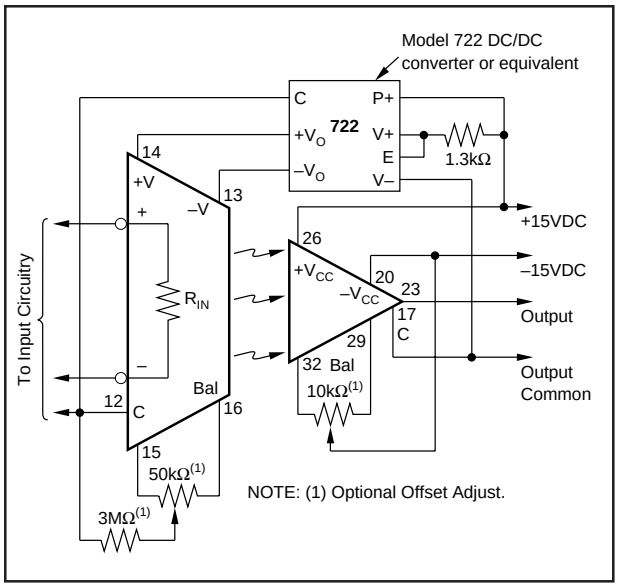
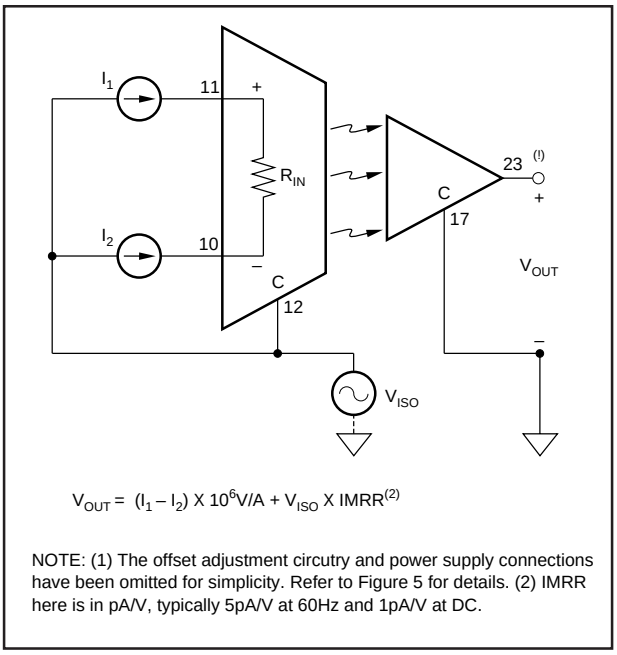
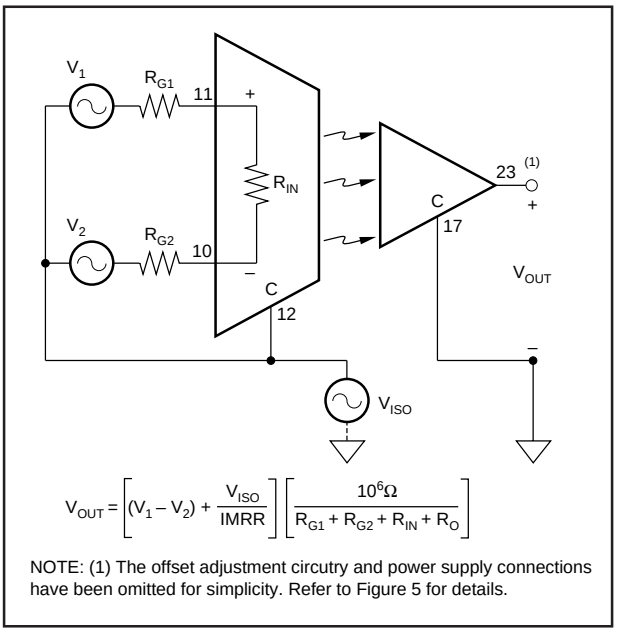


FIGURE 5. Power and Offset Adjust Connections.



$$V_{OUT} = (I_1 - I_2) \times 10^6 V/A + V_{ISO} \times IMRR^{(2)}$$

FIGURE 6a. 3650 with Differential Current Sources.



$$V_{OUT} = \left[(V_1 - V_2) + \frac{V_{ISO}}{IMRR}\right]\left[\frac{10^6\Omega}{R_{G1} + R_{G2} + R_{IN} + R_O}\right]$$

FIGURE 6b. 3650 with Differential Voltage Sources.

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with nondifferential inputs, the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used, it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers, A_1 and A_2, are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential, and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652, the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or $\pm I_R$ inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or $\pm I_R$ inputs. Figure 6c shows the +I and –I inputs used. If more input voltage protection is desired, then the $+I_R$ and $-I_R$ inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10ms rating of 3kV).

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{IN} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the

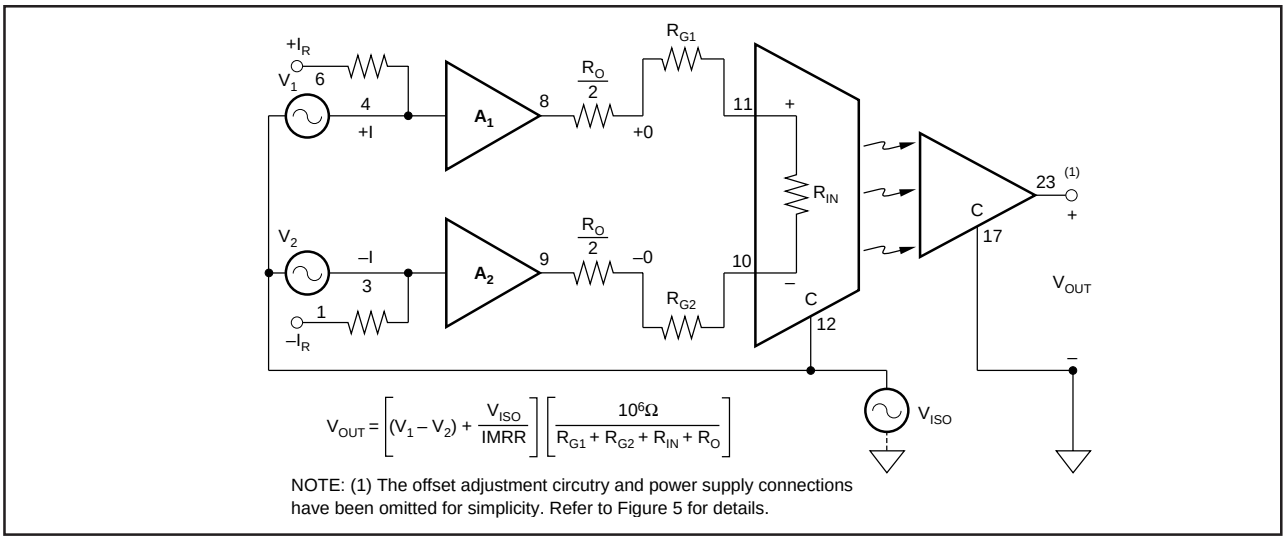


FIGURE 6c. 3652 with Differential Voltage Sources.

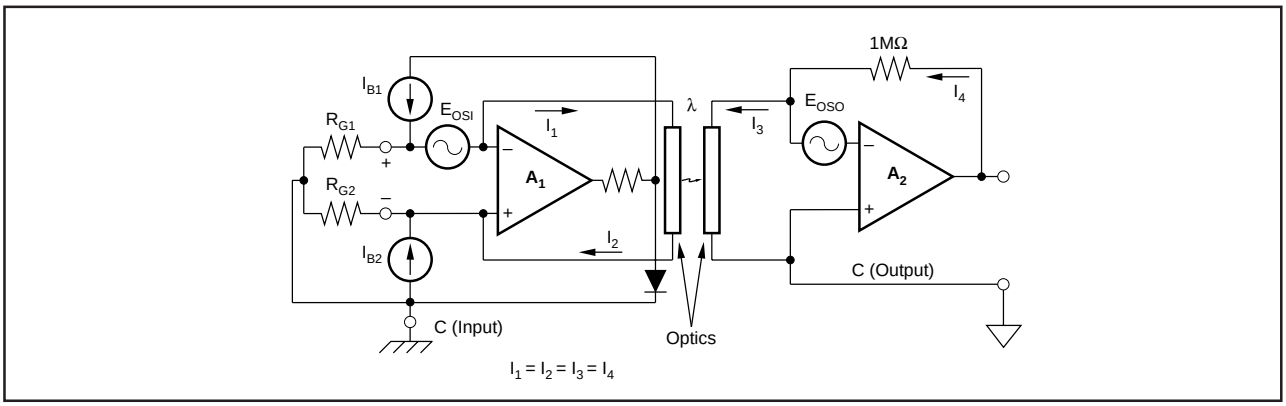


FIGURE 7. DC Error Analysis Model for 3650.

total output error voltage due to offset voltages and bias currents.

$$V_{OUT\text{-}TOTAL} = \frac{10^6}{R_{G1} + R_{G2}} [E_{OSI} + (I_{B1} R_{GI} - I_{B2} R_{G2})] + E_{OSO} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{OSI}$

then, for $R_{G1} = R_{G2}$, $V_{OUT} - I_B = \frac{10^6 I_{OS}}{2}$

This component of error is not a function of gain and is therefore included as a part of E_{OSO} specifications. The output errors due to the output stage bias current are also included in E_{OSO}. This results in a very simple equation for the total error:

$$V_{OUT\text{-}TOTAL} = \frac{10^6 E_{OSI}}{2R_{G1}} + E_{OSO} \text{ (for } R_{G1} = R_{G2}). \quad (2)$$

In summary, it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$$V_{OUT} \rightarrow \Delta V_{OUT}/\Delta T, \; E_{OSI} \rightarrow \Delta E_{OSI}/\Delta T, \text{ etc.}$$

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by:

$$E_N \text{ (RMS)} = \sqrt{(E_{NI}G)^2 + (E_{NO})^2}$$

where E_N (RMS) = Total output noise
E_{NI} = RMS noise of the input stage
E_{NO} = RMS noise of the output stage
$G = 10^6/(R_{G1} + R_{G2})$

E_{NO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE AND ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{OUT} = G\left[\frac{V_{CM}}{CMRR} + \frac{V_{ISO}}{IMRR}\right]$$

GUARDING AND PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted.

1. Use shielded twisted pair of cable at the input as with any instrumentation amplifier.
2. Care should be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR.
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

The armature current of the motor is converted to a voltage by the calibrated shunt R_S and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650s provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode impedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10ms pulse ratings of the $+I_R$ and $-I_R$ inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000Vpk continu-

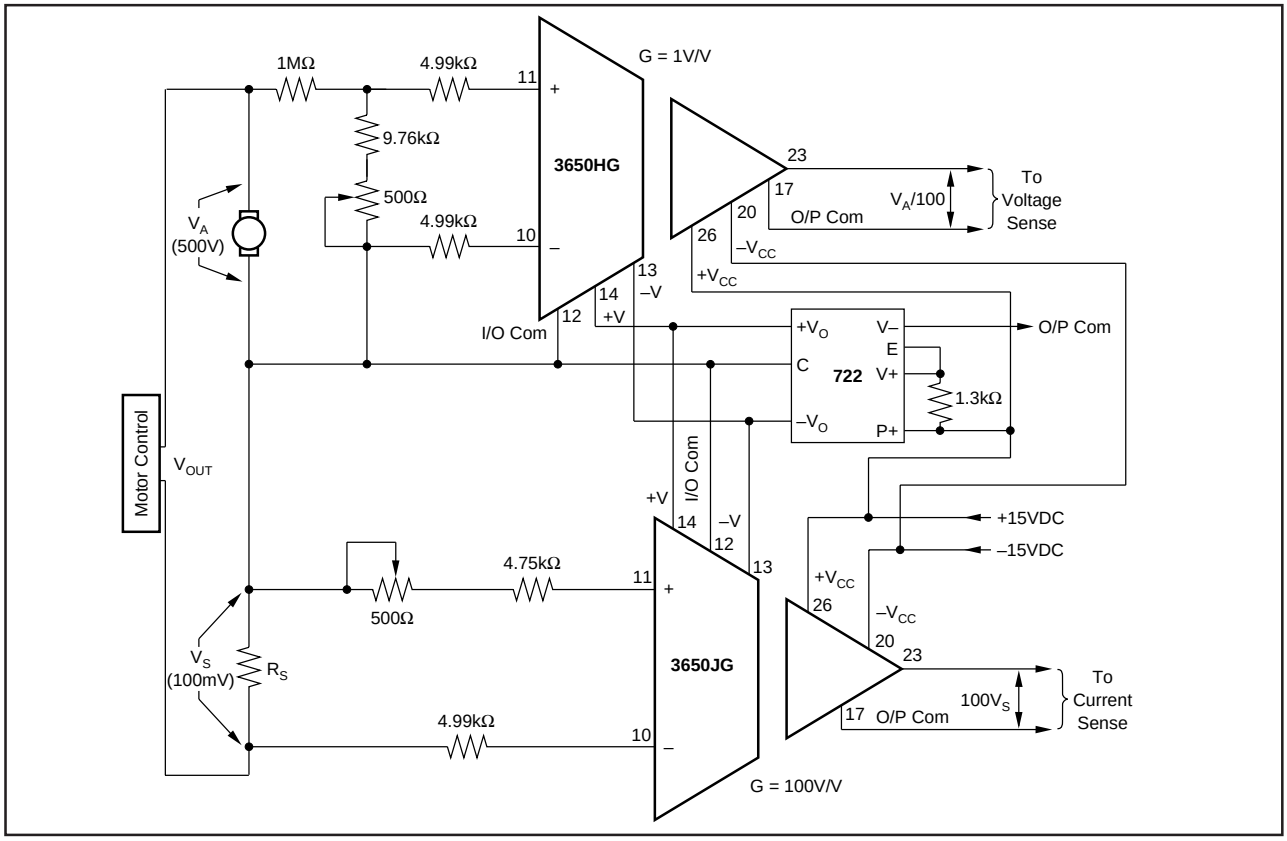


FIGURE 8. Isolated Armature Current and Voltage Sensor.

ous. The nonrecurrent pulse rating of the isolation barrier is 5000Vpk, since each unit is factory tested at 5000Vpk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3652s can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V 60Hz would still be less than 2µA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

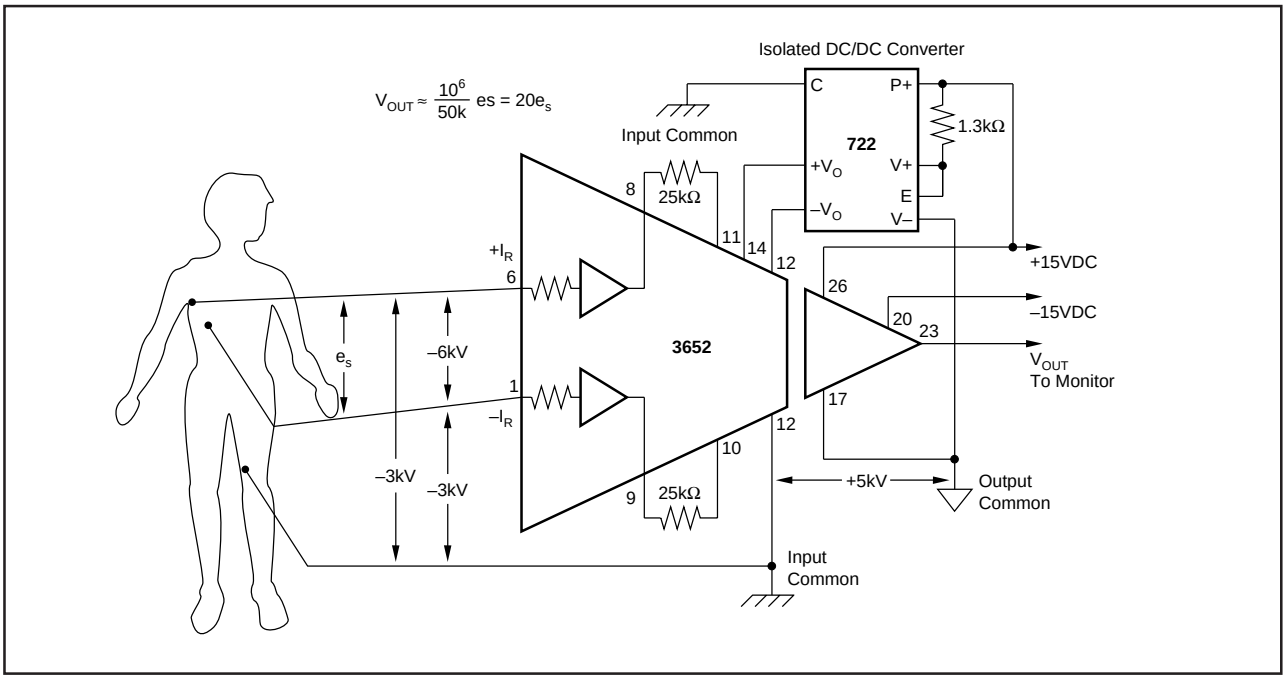


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

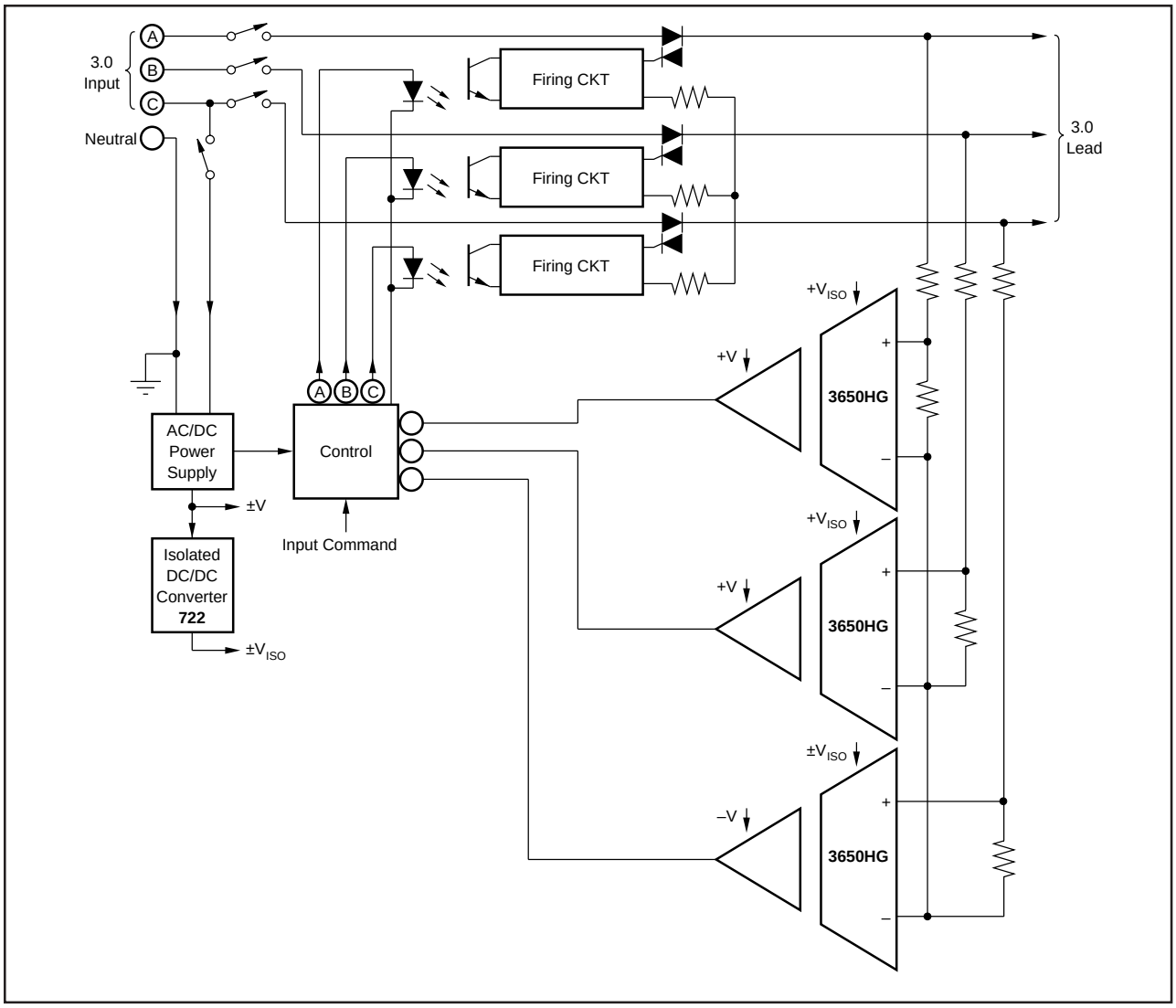


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
3650HG	NRND	CDIP	JNC	32	10	TBD	Call TI	N / A for Pkg Type
3650JG	NRND	CDIP	JNC	32	10	TBD	Call TI	N / A for Pkg Type
3650KG	NRND	CDIP	JNC	32	10	TBD	Call TI	N / A for Pkg Type
3650MG	NRND	CDIP	JNC	32	10	TBD	Call TI	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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